SW 5 - VHDL Adder

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Section 003L

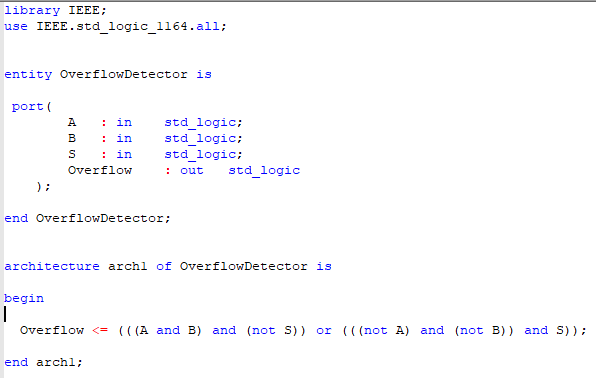
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**Overview**

VHDL is a ‘coding’ language used to design circuits that would otherwise be difficult to build in programs, such as LogicWorks, or assemble with real-life hardware. It allows users to experiment with and test circuits before building anything in real life, to see if the logic functions in an optimal setting, to account for confounding variables like noise, misplace wires, faulty integrated chips, or many other issues that come from building a circuit in real life. It is also much more cost-effective than purchasing the materials to build circuits to test because it requires no resources other than the computer it is running on.

**VHDL Code**



**Question**

Since you have built a similar circuit in the Adders assignment, which design method did you prefer for constructing the 4-bit adder with LogicWorks: writing VHDL modules or connecting discrete gates? Why?

I preferred the VHDL method, once I figured out how to use VHDL, because I am more experienced with coding than with wiring circuits and found it easier. I do like how the circuit looks in LogicWorks once it’s working because I like seeing a visual design of the logic more than reading words and symbols, but writing code is easier than making a circuit for the process rather than after-the-fact.